REMARKS

This amendment is in response to the Office Action dated April 17, 2006. Claims 1-19 are pending. Claims 1, 9, 15 and 19 are currently amended to further clarify the invention. Applicants respectfully request reconsideration of the application in view of the following remarks submitted in support thereof.

Rejections under 35 U.S.C. § 101

Claims 1-4, 9-19 were rejected under 35 USC 101 because the claimed invention was directed to non-statutory subject matter. Claims 1, 9, 15 and 19 have been amended to include a tangible result. Based on the now amended claims, the Applicants request the rejections under 35 USC 101 of claims 1-4, 9, 11-12, 14-18 be withdrawn.

Claims 9-14 were regarded as directed to software. Claim 9 has now been amended to include the hardware that executes the software. Based on the now amended claim, the Applicants request the 101 rejection of claims 9-14 be withdrawn.

Claims 15-19 were regarded as directed to non-statutory computer readable medium. Claims 15 and 19 have been amended to include a tangible statutory computer-readable medium. Based on the now amended claims 15 and 19, the Applicants request the 101 rejection of claims 15-19 be withdrawn. Applicants respectfully disagree with the Examiner's characterization of these claims as the original computer readable medium claims were directed to statutory subject matter. MPEP 2106 (IV) (B) (1) (a) explicitly states that a claimed computer readable medium encoded with a computer program is a computer element which defines structural and functional interrelationships between the computer program and the rest of the computer, which permit the computer program's functionality to be realized, and is thus statutory. However, in an effort to further move prosecution along, the Applicants have amended the claims.

Rejections under 35 U.S.C. § 112

Claims 5, 10 and 19 were rejected under 112, second paragraph for having insufficient antecedent basis. With reference to claim 5, Applicants would like to point out that the now amended independent claim 1 from which claim 5 directly depends on includes "method operations" in the preamble and the limitation in claim 5 has antecedent basis in claim 1 for the unacceptable comparison of the signals.

With reference to claim 10, the logic for identifying a cause in the now currently amended claim 10 has antecedent basis as the now amended independent claim 9 from which claim 10 directly depends includes such limitation.

With reference to claim 19, "the program instructions for identifying a cause" has sufficient antecedent basis as the now amended independent claim 15 includes such limitation.

Based on the above argument, the Applicants request 112 rejection be withdrawn for claims 5, 10 and 19.

Rejections under 35 U.S.C. § 102:

Claims 1-6, 9-12 and 14-19 were rejected under 102(e) as being anticipated by Shimogori et al. (U.S. Patent Application No. 2002/0152061A1) (Shimogori). This rejection is respectfully traversed.

Shimogori discloses a data processing system and method for simulating operation of a processor for an application program including instruction sets. The operation of defining a library of components for a processor in Shimogori that the Examiner is pointing to in paragraph [0083] is actually a library of instruction sets and not the library of components that is claimed in the claimed invention. The library of components, according to claims 1, 9, and 15 of the present invention, includes high level chip components. (*See page 15, lines 2-*

5). Applicants respectfully request that the Examiner specify how instruction sets disclose a hardware component such as, Memory or some other functional block.

The operation of defining interconnections for a set of pipelined processors including the processor of Shimogori actually refers to interconnections of various pipeline stages within the components of a single processor used in executing a standard instruction set. As mentioned in paragraph [0047] of Shimogori, a construction composed of a Fetch Unit 5, the Processing Unit 2, the code RAM 4 and the data RAM 15 are all components within a single processor as opposed to a set of pipelined processors of the claimed invention. As described in the claimed invention, the pipelined processors of the claimed invention include a plurality of processors, each of the processors equipped with input socket interface, star processor, output socket interface and hardware accelerator with the output socket interface of a first processor in communication with input socket interface of a second processor. Accordingly, Shimogori fails to teach this feature.

The operation of combining the library of components and the interconnections for the set of pipelined processors of Shimogori that the Examiner has pointed out in paragraph [0083] actually refers to a library program that provides functions to convert *instruction sets* into information that is managed by a simulation program. This is not the same as the claimed invention as specified in claims 1, 9, and 15. As mentioned above, a library of instruction sets is not the same as library of components. Accordingly, it cannot be reasonably asserted that Shimogori discloses generation of a processor circuit by combining the library of components with the interconnections for the pipelined processors, as discussed above Shimogori neither teaches the library components nor the interconnections for the pipelined processors.

Applicants respectfully submit that Shimogori does not disclose generating a code representation of a model of the set of pipelined processors of the claimed invention. The

code representation of a model of Shimogori actually defines a model of the different stages of the instruction set within a single processor such as a Fetch and Decode stage, an Execution stage and a Write back stage. If the Examiner maintains this rejection, Applicants respectfully request that the examiner explain how a model of different stages of instruction sets within a single processor discloses a model of a set of pipelined processors.

Further, Shimogori does not suggest or teach comparing signals represented by the code representation to signals generated by the processor circuit. According to Shimogori, the "comparison" is to verify when a particular bit pattern from a signal stream is executed. Shimogori does not suggest or teach comparing the signals generated by the processor circuit to the signals generated by the code representation of the processor circuit. In the reference paragraph of Shimogori pointed by the Examiner (paragraph [0062]), there is no mention of signals generated let alone signals generated by a processor circuit or signals generated by code representation of the processor circuit and comparison of these signals. As a result, Shimogori does not suggest or teach comparison of signals. Applicants respectfully request that the examiner clarify where Shimogori teaches the comparison of signals representing a code representation and signals generated by the processor circuit.

Shimogori does not suggest or teach identifying a cause of the unacceptable comparison of the signals at a block level of the processor circuit. Since there are no signals generated in Shimogori, then there can be no comparison of signals. In fact, paragraph [0090] suggests that the only verification that is done is to determine if the test functions have been properly ported in the program that has been compiled by the pcc 101. This, according to Shimogori, is to investigate what parts of the code can be sped up through a conversion to hardware. Shimogori simply does not suggest or teach identifying a cause of the unacceptable comparison of signals at a block level of the processor circuit as suggested by the claimed invention. In fact, Shimogori does not mention any block level processing. The

cause of unacceptable comparison of signals at a block level of the processor circuit, according to the claimed invention, is useful in pinpointing the location of the problem, which is useful in looking at errors in chunks thereby resulting in efficient correction of errors. (*See page 14, lines 4-8).*

Accordingly, Shimogori does not teach the above embntioed features and the Applicants respectfully request that the rejections of claim 1, 9, and 15 be withdrawn for at least the above stated reasons.

With reference to claim 6, Shimogori does not teach identifying a block level location having an error from a first simulation. In fact, Shimogori does not teach identifying an error anywhere in the cited section. Applicants respectfully request that the Examiner specify where an error is disclosed in the cited section. As a result, Applicants submit that Shimogori does not suggest or teach inserting a patch into a thread specific to the block level location of the error. Shimogori specifies conversion of code to hardware to speed the process up. This has nothing to do with inserting a patch into an error location and then executing a second simulation to determine signal level location of the error using the information generated by the inserted patch. Finally, since there are no errors detected or a patch inserted, Shimogori can not suggest correcting a code representation of a processor associated with the error. As a result, the elements of claim 6 are not disclosed in Shimogori. Based on the arguments, the Applicants request the withdrawal of rejection of claim 6.

With reference to claims 2-5, 10-12, 14, and 16-19 are dependent on independent claims 1, 6, 9 and 15. Based on the above arguments, Applicants request the withdrawal of the rejections on claims 2-5, 10-12, 14, and 16-19.

Rejections under 35 U.S.C. § 103:

Claims 7, 8 and 13 were rejected under 35 U.S.C. § 103(a), as being unpatentable over Shimogori in view of Shridhar et al. (U.S. Patent No. 5,815,714) (Shridhar). This rejection is respectfully traversed.

Claims 7, 8, and 13 depend from claims 6 and 9. Shridhar does not cure any of the above mentioned deficiencies of Shimogori. Based on the arguments presented, Applicants request that the 103 rejections be withdrawn and claims 7, 8 and 13 be allowed.

A Notice of Allowance is respectfully requested. If the Examiner has any questions concerning the present Amendment, the Examiner is kindly requested to contact the undersigned at (408) 774-6921. If any other fees are due in connection with filing this Amendment, the Commissioner is also authorized to charge Deposit Account No. 50-0805 (Order No. ADAPP222). A duplicate copy of the transmittal is enclosed for this purpose.

Respectfully submitted,
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